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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,747	07/16/2003	Bruce Rosenthal	AME-006	1814

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EXAMINER	
PATEL, RAJNIKANT B	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,747	ROSENTHAL, BRUCE	
	Examiner	Art Unit	
	Rajnikant B Patel	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/16/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neill et al. (U.S. Patent # 4,851,953) in combination with Dooley et al. (U.S. Patent # 6,292,050) and Gilbert et al. (U.S. Patent # 5,847,614).

O'Neill et al. disclose the claimed invention a bandgap reference voltage circuit (figure 2), including Brokaw cell and first and second transistor (figure 2, item 202,204,206, and 208). However O'Neill et al. does not disclose the utilization of the technique for a modified Brokaw cell and cascade amplifier. Gilbert et al. teaches the utilization of the similar technique for modified Brokaw cell (column 8, line 25-45) and Dooley et al. teaches the utilization of the similar technique for a cascode amplifier. It would have been obvious one having an ordinary skill in the art at the time the invention was made to modify O'Neill et al.'s bandgap reference circuit by utilizing the technique taught by Gilbert et al. and Dooley et al. for the purpose of providing a current and compensated voltage reference that is capable of operating from a power supply voltage as low as approximately 1.3 volts. Further O'Neill et al. in combination with Dooley et al. disclose the technique of cascade amplifier includes a bias circuit (column 3, line 15-50), CMOS technology (column 2, line 30-40) and resistance and current source (claim 1).

3. Claims 3,8,10,12-14 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neill et al. (U.S. Patent # 4,851,953) in combination with Dooley et al. (U.S. Patent # 6,292,050), Guibert et al. (U.S. Patent # 5,847,614) and further in combination with Gramegna (U.S. patent # 6,392,490).

O'Neill et al. in combination with Dooley et al. and Gilbert et al. discloses claimed inventions explained in the claims 1-4 and 7-11, above except the utilization of the technique for an output shunt device. Gramegna et al. teaches the utilization of the similar technique for an output shunt regulation (Abstract line 10-15). It would have been obvious one having an ordinary skill in the art at the time the invention was made to modify O'Neill et al.'s bandgap reference circuit by utilizing the technique taught by Gilbert et al., Dooley et al. and Gramegna et al. for the purpose of providing a high-precision bias circuit.

In regards to claims 3,10,14 and 21 O'Neill et al. in combination with Dooley et al. and Gilbert et al. discloses claimed inventions explained in the claims 1-4 and 7-11, above, except the utilization of lateral PNP and NPN transistors. It would have been obvious one having an ordinary skill in the art at the time the invention was made to utilized PNP and NPN transistor, since it has been held to be within the general skill in the art to select a known material on the basis of its suitability for intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

4. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neill et al. (U.S. Patent # 4,851,953) in combination with Dooley et al. (U.S. Patent #

6,292,050), Gilbert et al. (U.S. Patent # 5,847,614) and further in combination with Fujimori (U.S. patent # 5,966,005)

O'Neill et al. in combination with Dooley et al. and Gilbert et al. discloses claimed inventions explained in the claims 1-4 and 7-11, above except the utilization of the technique for NMOS and PMOS transistor configuration. Fujimori teaches the utilization of the similar technique for NMOS and PMOS transistor configuration (figure 9). It would have been obvious one having an ordinary skill in the art at the time the invention was made to modify O'Neill et al.'s bandgap reference circuit by utilizing the technique taught by Gilbert et al., Dooley et al. and Fujimori for the purpose of providing a high-precision bias circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rajnikant B Patel whose telephone number is 571-272-2082. The examiner can normally be reached on 6.30-5.00; m-f.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rajnikant B Patel
Primary Examiner
Art Unit 2838

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